Development Board EPC9068 Quick Start Guide

EPC8010

100 V Half Bridge with Sync FET Bootstrap Gate Drive

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9068 development board is a 100 V maximum device voltage, 2.7 A maximum output current, half bridge with onboard gate drives, featuring the EPC8010 enhancement mode (eGaN®) field effect transistor (FET). The gate driver has been configured with a synchronous FET bootstrap circuit featuring the EPC2038 eGaN FET that eliminates high side device losses induced by the reverse recovery losses of the internal bootstrap diode of the gate driver. The purpose of this development board is to simplify the evaluation process of the EPC8010 eGaN FET by including all the critical components on a single board that can be easily connected into any existing converter. The inclusion of the synchronous FET bootstrap circuit enables significant increase in operating frequency capability of the half bridge circuit.

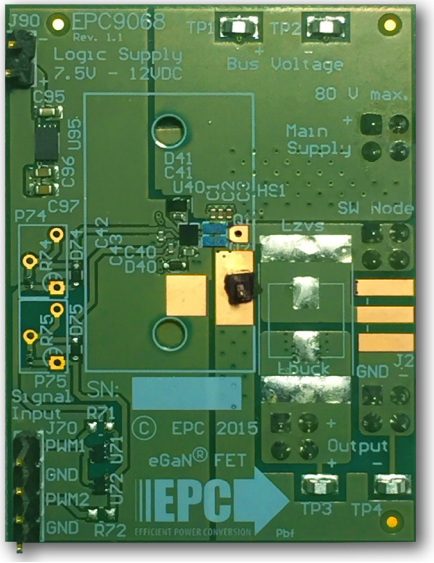
The EPC9068 development board is 2" x 1.5" and has two EPC8010 eGaN FETs in a half bridge configuration using Texas Instruments LM5113 gate driver with supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. The board includes pads for the inclusion of customer components to facilitate testing in a Buck converter or ZVS class-D amplifier configurations. A complete block diagram of the circuit is given in figure 1.

For more information on the EPC8010 and EPC2038 eGaN FETs please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC9068

Symbol	Parameter	Conditions	Min	Max	Units
V_{DD}	Gate Drive Input Supply Range		7.5	12	V
V_{IN}	Bus Input Voltage Range			80*	V
V_{OUT}	Switch Node Output Voltage			100	V
I_{OUT}	Switch Node Output Current			2.7*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	40		ns
	Minimum 'Low' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	160#		ns

**Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.*
 # Limited by time needed to 'refresh' high side bootstrap supply voltage.



EPC9068 development board

QUICK START PROCEDURE

Development board EPC9068 is easy to set up to evaluate the performance of the EPC8010 eGaN FET. Refer to figure 2 for proper connect and measurement setup and follow the procedure below:

1. Configure the board for either ZVS class-D operation OR Buck converter operation.
2. With power off, connect the input power supply bus to +VIN (J1) and ground / return to –VIN (J4).
3. For ZVS class-D operation, with power off, connect a HF load to the HF output (RF-J2 OR Vsw-J3 and GND-J4). For Buck converter operation, with power off, connect a DC load to the DC output (+VOUT-J5 and GND-J4).
4. With power off, connect the gate drive input to +VDD (J90, Pin-1) and ground return to –VDD (J90, Pin-2).
5. With power off, connect the input PWM control signal to PWM (J70, Pin-1) and ground return to either Pin-2 or Pin-4 of J70.
6. Turn on the gate drive supply – make sure the supply is within the 7.5 V and 12 V range.
7. Turn on the controller / PWM input source and probe switching node to observe switching operation.
8. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 52 V on VOUT). Increase voltage slowly while monitoring operation to ensure the FETs are operating within their datasheet parameters.
9. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
10. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node, care must be taken to avoid long ground leads. Measure the switch node by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminal provided. See figure 3 for proper scope probe technique.

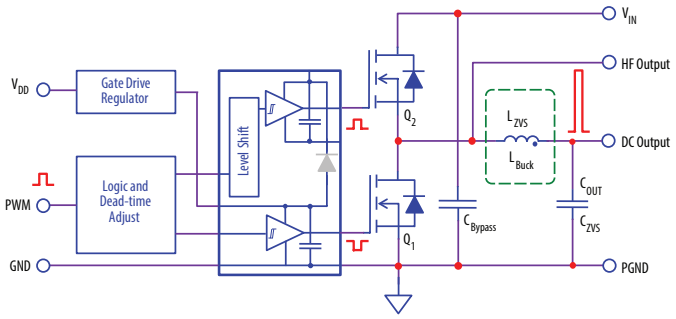


Figure 1: Block diagram of EPC9068 development board

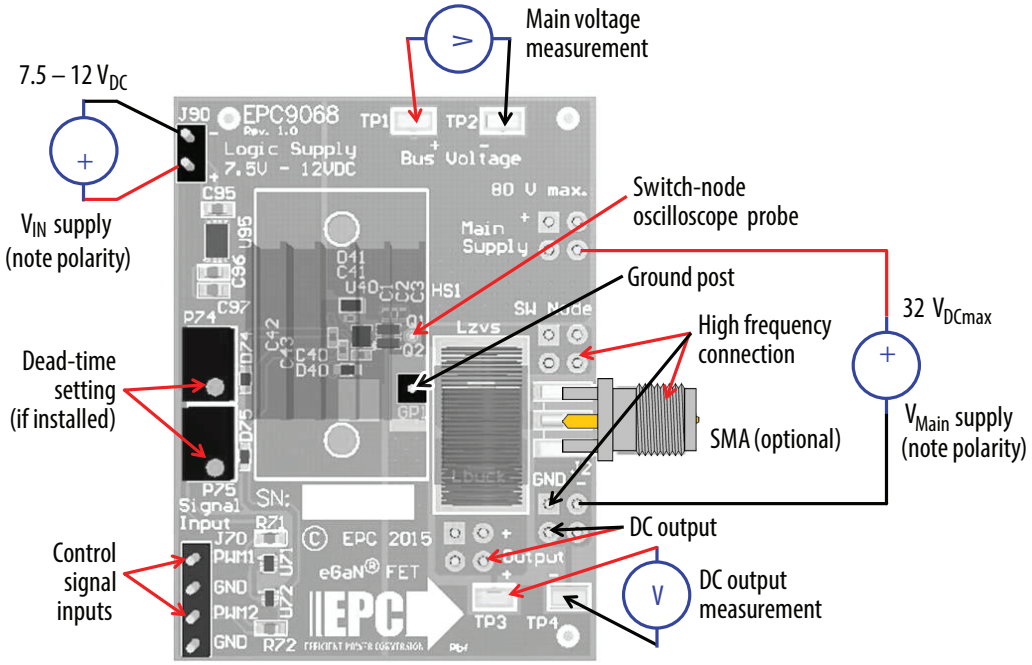


Figure 2: Proper connection and measurement setup

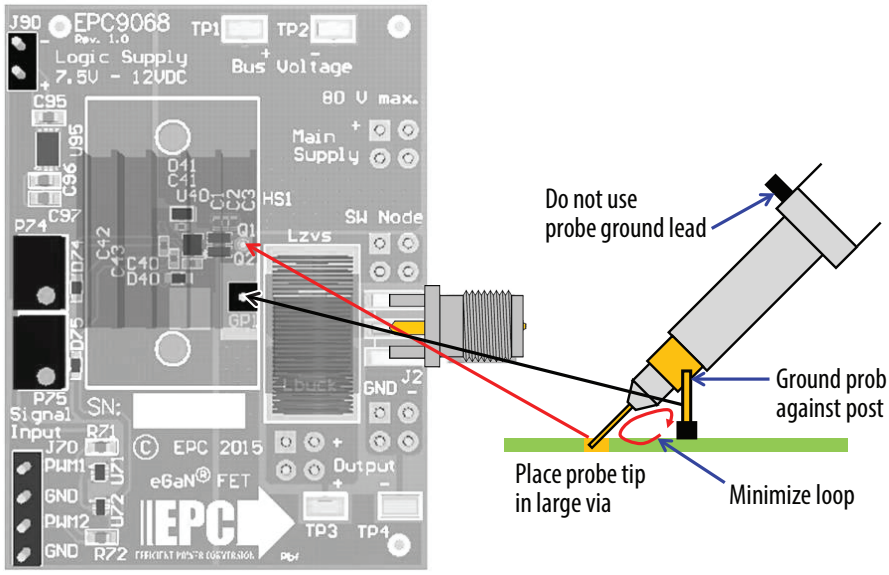


Figure 3: Proper measurement of the switch node

THERMAL CONSIDERATIONS

The EPC9068 development board showcases the EPC8010 eGaN FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9068 is intended for bench evaluation with low ambient temperature and convection cooling.

The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9068 development board does not have any current or thermal protection on board.

Table 2: Bill of Materials - Amplifier Board

Item	Qty	Reference	Part Description	Manufacturer/Part Number
1	1	C40	Capacitors, Ceramic, 4.7 µF, 10 V, ±20%, X5R	Samsung, CL05A475MP5NRNC
2	3	C4, C5, C6	Capacitors, Ceramic, 1.0 µF, 100 V, ±10%, X7S	TDK, C2012X7S2A105K125AB
3	3	C95, C96, C97	Capacitors, Ceramic, 1.0 µF, 25 V, ±10%, X5R	Murata, GRM188R61E105KA12D
4	2	C71, C72	Capacitors, Ceramic, 100 nF, 25 V, ±10%, X7R	TDK, C1005X7R1E104K050BB
5	2	C41, C44	Capacitors, Ceramic, 100 nF, 16 V, ±10%, X7R	Murata, GRM155R71C104KA88D
6	1	C45	Capacitors, Ceramic, 22 nF, 25 V, ±10%, X7R	TDK, C1005X7R1E223K050BB
7	3	C1, C2, C3	Capacitors, Ceramic, 10 nF, 100 V, ±20%, X7S	TDK, C1005X7S2A103M050BB
8	2	C42, C43	Capacitors, Ceramic, 22 pF, 50 V, ±5%, NPO	TDK, C1005C0G1H220J050BA
9	1	R46	Resistors, 27 KΩ, ±1%, 1/10 W	Panasonic, ERJ-2RKF2702X
10	1	R70	Resistors, 10.0 KΩ, ±1%, 1/10 W	Panasonic, ERJ-6ENF1002V
11	1	R74	Resistors, 270 Ω, ±1%, 1/10 W	Panasonic, ERJ-2RKF2700X
12	1	R75	Resistors, 82 Ω, ±1%, 1/10 W	Panasonic, ERJ-2RKF82R0X
13	1	R45	Resistors, 20 Ω, ±1%, 1/16 W	Stackpole, RMCF0402FT20R0
14	1	R44	Resistors, 4.7 Ω, ±1%, ±/16 W	Yageo, RC0402FR-074R7L
15	3	D45, D74, D75	Diodes, Schottky Diode, 30 V, VF=370 mV @ 1 mA, 30 mA	Diodes Inc, SDM03U40-7
16	1	D40	Diodes, Schottky, 100 V, 0.2 A, VF=1 V @ 200 mA	ST Microelectronics, BAT41KFILM
17	1	D41	Diodes, Zener, 5.1 V, 150 mW ±5%	Bourns Inc., CD0603-Z5V1
18	1	Q44	eGaN® FET, 100 V, 500 mA, $R_{DS(on)}$=2.1 Ω @ 50 mA, 5V	EPC, EPC2038
19	2	Q1, Q2	eGaN® FET, 100bV, 3.4 A, $R_{DS(on)}$=160 mΩ @ 500 mA	EPC, EPC8010
20	1	U95	IC's, 5 V LDO, 250 mA, up to 16 V_{IN}, $V_{dropout}$=0.33 V @ 250 mA	Microchip, MCP1703T-5002E/MC
21	1	U40	IC's, Gate Driver, 5.2 VDC, 1.2 A, 4.5 V to 5.5 V	Texas Instruments, LM5113TME/NOPB
22	1	U72	IC's, Logic 2 NAND Gate, 1.65 V to 5.5 V, ± 24 mA	Fairchild, NC7SZ00L6X
23	1	U71	IC's, 2 input AND Gate, Tiny Logic, 1.65 V to 5.5 V, ± 32mA	Fairchild, NC7SZ08L6X
24	4	TP1, TP2, TP3, TP4	Test Point, Test Point Subminiature	Keystone, 5015
25	0.19	J70, J90, GP1 (See Note 1)	Headers, Male Vertical, 36 Pin. 230" Contact Height, .1" Center Pitch	FCI, 68001-236HLF
26	4	J1, J3, J4, J5	Headers, 2 Rows by 2 Pins .1" Male Vertical, .1" Center Pitch	TE Connectivity, 5-146256-2

Optional Components

Item	Qty	Reference	Part Description	Manufacturer/Part Number
1	1	C7	Capacitors, DNP, Ceramic, 1.0 µF, 100 V, ±10%, X7S	TDK, C2012X7S2A105K125AB
2	1	C46	Capacitor, DNP, Ceramic, 100 nF, 16 V, ±10%, X7R	Murata, GRM155R71C104KA88D
3	3	R71, R72, R73	Resistor, DNP, 0 Ω, 1/10 W, Jumper	Panasonic, ERJ-3GEY0R00V
4	2	P74, P75	Potentiometer, DNP, Multi-turn Potentiometer, 1 kΩ, ±10%, 1/4 W, 12 Turn Top Adjustment Small	Murata, PV37W102C01B00
5	1	Lbuck	Inductor, DNP, 10 µH, ±20%, 3.5 A, 33 mΩ, Resonance=40 MHZ, Frequency Tested=100 KHz	Würth, 744314101
6	1	Lzvs	Inductor, DNP. 500 nH, Q=180, 50 MHZ, DCR=16.5 mΩ, Irms=4.3 A	Coilcraft, 2929SQ-501JEB
7	1	D44	Diodes, DNP, Schottky Diode, 30 V, VF=370 mV @ 1 mA, 30 mA	Diodes Inc, SDM03U40-7
8	1	J2	Connector, DNP, RP-SMA Plug, 50 Ω	Linx, CONREVSMA013.062
9	1	HS1	Hardware, DNP, W= (0.590") 15 mm, by L= (0.590") 15 mm, H= (0.374") 9.5 mm, 26.2°C/W @ 200 LFM	Advanced Thermal Solutions, ATS-54150D-C2-R0

Note 1 (36 pin Header to be cut as follows) J70 cut 4 pins used, J90 cut 2 pins used, GP1 cut 1 pin used

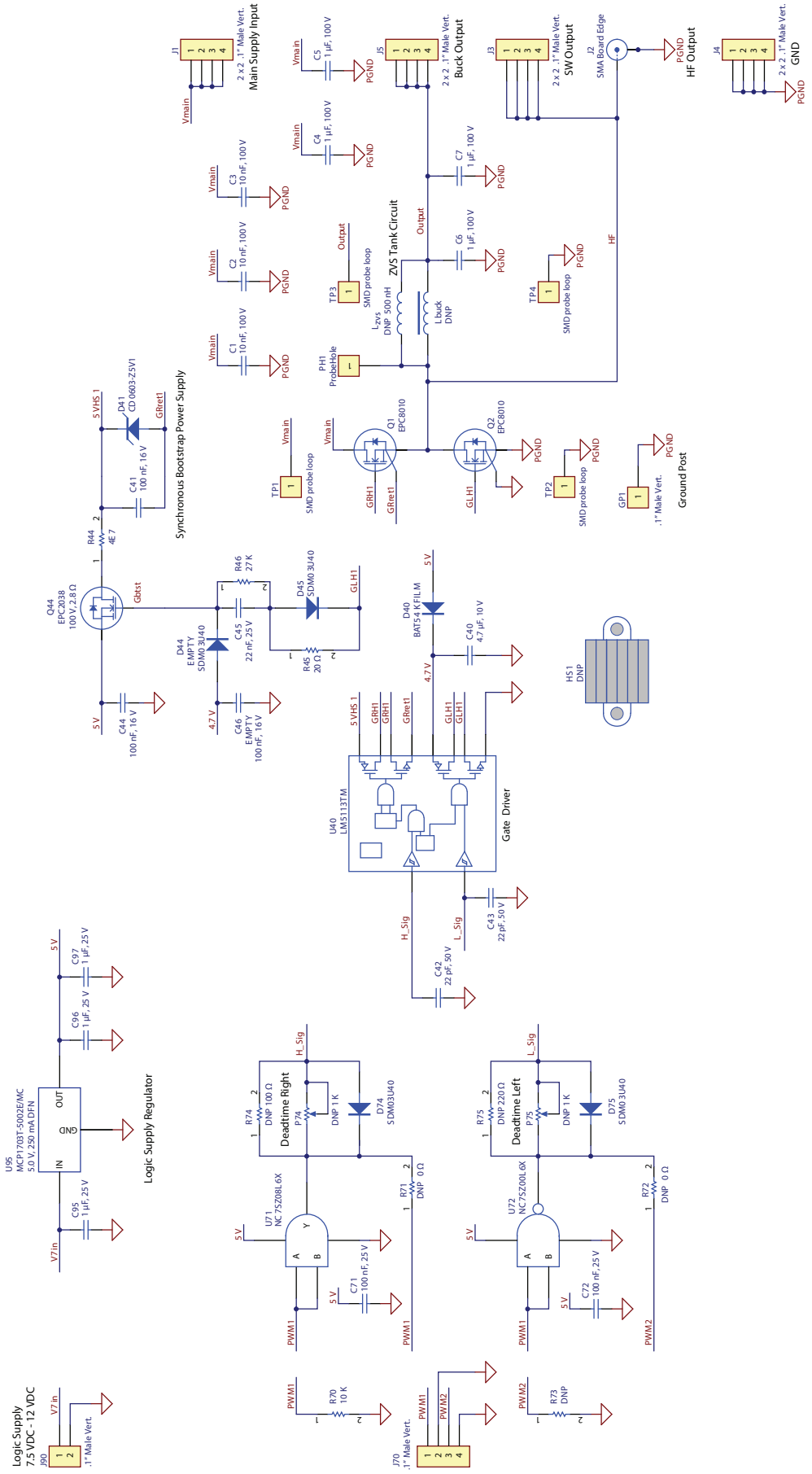


Figure 4: EPC9068 - Schematic

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